REMARKS

All rights are reserved to the original claimed subject matter. The claims have been amended to reduce the filing fees and to restate the inventive subject matter in clear terms. None of the amendments are intended to narrow any element of the claims as they stood prior to amendment. Examination of the application as amended is respectfully requested.

Respectfully submitted,
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APPENDIX OF MARKED UP VERSION OF CLAIMS

1(Amended). A semiconductor memory chip module [having] comprising a first memory chip (4) of a first type, a second memory chip (6) of a second type, and an electric connection (14, 16) between the first and second memory chips (4, 6), [characterized in that] wherein the memory chips (4, 6) are disposed one above the other in different levels and connected by vertical chip interconnections (14, 16).

2(Amended). A chip module according to claim 1, [characterized in that] wherein memory cells (C4) of the first memory chip (4) are firmly allocated to certain memory cells (C6) of the second memory chip (6), and the mutually allocated memory cells (C4, C6) are directly interconnected electrically.

3(Amended). A chip module according to claim 1 [or 2, characterized in that], wherein the first type corresponds to a nonvolatile memory, for example EEPROM, and the second type to a volatile memory, for example SRAM.

4(Amended). A chip module according to [any of claims 1 to 3, characterized in that] claim 1, wherein at least one further chip (8, 16) is provided in a further level.

5(Amended). A chip module according to claim 4, [characterized in that] wherein the further chip contains decoder circuits (10, 12) for the memory chips (4, 6).

6(Amended). A chip module according to [any of claims 1 to 5, characterized in that] claim 1, wherein an energy buffer is formed in at least one of the levels.

7(Amended). A chip module according to claim 6, [characterized in that] wherein the energy buffer is formed as an integrated buffer capacitor (20).

8(Amended). A chip module according to [any of claims 1 to 7] claim 1, formed for a smart card.

9(Amended). A smart card having a semiconductor memory chip module according to [any of claims 1 to 8] claim 1.

APPENDIX OF CLAIMS

1(Amended). A semiconductor memory chip module comprising a first memory chip (4) of a first type, a second memory chip (6) of a second type, and an electric connection (14, 16) between the first and second memory chips (4, 6), wherein the memory chips (4, 6) are disposed one above the other in different levels and connected by vertical chip interconnections (14, 16).

2(Amended). A chip module according to claim 1, wherein memory cells (C4) of the first memory chip (4) are firmly allocated to certain memory cells (C6) of the second memory chip (6), and the mutually allocated memory cells (C4, C6) are directly interconnected electrically.

3(Amended). A chip module according to claim 1, wherein the first type corresponds to a nonvolatile memory, for example EEPROM, and the second type to a volatile memory, for example SRAM.

4(Amended). A chip module according to claim 1, wherein at least one further chip (8, 16) is provided in a further level.

5(Amended). A chip module according to claim 4, wherein the further chip contains decoder circuits (10, 12) for the memory chips (4, 6).

6(Amended). A chip module according to claim 1, wherein an energy buffer is formed in at least one of the levels.

7(Amended). A chip module according to claim 6, wherein the energy buffer is formed as an integrated buffer capacitor (20).

8(Amended). A chip module according to claim 1, formed for a smart card.

9(Amended). A smart card having a semiconductor memory chip module according to claim 1.

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